LISTING OF THE CLAIMS

1. (Original) A method of performing multi-level comma detection and alignment on an unaligned data stream, the method comprising:

receiving the unaligned data stream;

comparing each N consecutive bits in the unaligned data stream with a predetermined byte value having N bits, where N is an integer;

aligning, when a first set of N consecutive bits matches the predetermined byte value, the unaligned data stream based on a position of the predetermined byte value within the unaligned data stream to provide a partially aligned data stream;

comparing Q consecutive data bytes in the partially aligned data stream with a predetermined sequence of byte values, where Q is an integer; and

aligning, when a first set of Q consecutive bytes matches the predetermined sequence of byte values, the partially aligned data stream based on a position of the first set of Q consecutive bytes within the partially aligned data stream to provide a fully aligned data stream.

2. (Original) The method of Claim 1, wherein comparing Q consecutive data bytes comprises comparing each Q consecutive data bytes within the partially aligned data stream at least until a first match is found.

3. (Original) The method of Claim 1, further comprising generating a second value identifying a position of the predetermined byte value within the partially aligned data stream, and wherein comparing Q consecutive data bytes comprises utilizing the second value to identify a comparison to perform that includes the predetermined byte value.

4. (Original) The method of Claim 1, wherein aligning the unaligned data stream comprises aligning the unaligned data stream with preceding and following edges of the predetermined byte value.

5. (Original) The method of Claim 4, wherein aligning the partially aligned data stream comprises aligning the partially aligned data stream with a center point of the predetermined sequence of byte values.

6. (Original) The method of Claim 1, wherein aligning the partially aligned data stream comprises aligning the partially aligned data stream with a center point of the predetermined sequence of byte values.

7. (Original) The method of Claim 1, wherein N is eight.

8. (Original) The method of Claim 7, wherein Q is four.

9. (Original) The method of Claim 1, wherein Q is four.

10. (Original) The method of Claim 1, wherein:

the unaligned data stream conforms to a SONET communications standard;

the predetermined byte value is A2 as defined by the SONET standard; and

the predetermined sequence of byte values is A1_A1_A2_A2 as defined by the SONET standard.

11. (Original) A circuit, comprising:

means for receiving an unaligned data stream;

means for comparing each N consecutive bits in the unaligned data stream with a predetermined byte value having N bits, where N is an integer;

means for aligning, when a first set of N consecutive bits matches the predetermined byte value, the unaligned data stream based on a position of the predetermined byte value within the unaligned data stream to provide a partially aligned data stream;

means for comparing Q consecutive data bytes in the partially aligned data stream with a predetermined sequence of byte values, where Q is an integer; and

means for aligning, when a first set of Q consecutive bytes matches the predetermined sequence of byte values, the partially aligned data stream based on a position of the first set of Q consecutive bytes within the partially aligned data stream to provide a fully aligned data stream.

12. (Original) The circuit of Claim 11, wherein the means for comparing Q consecutive data bytes comprises means for comparing each Q consecutive data bytes within the partially aligned data stream at least until a first match is found.

13. (Original) The circuit of Claim 11, further comprising means for generating a second value identifying a position of the predetermined byte value within the partially aligned data stream, and wherein the means for comparing Q consecutive data bytes comprises means for utilizing the second value to identify a comparison to perform that includes the predetermined byte value.

14. (Original) The circuit of Claim 11, wherein the means for aligning the unaligned data stream comprises means for aligning the unaligned data stream with preceding and following edges of the predetermined byte value.

15. (Original) The circuit of Claim 14, wherein the means for aligning the partially aligned data stream comprises means for aligning the partially aligned data stream with a center point of the predetermined sequence of byte values.

16. (Original) The circuit of Claim 11, wherein the means for aligning the partially aligned data stream comprises means for aligning the partially aligned data stream with a center point of the predetermined sequence of byte values.

17. (Original) The circuit of Claim 11, wherein N is eight.

18. (Original) The circuit of Claim 17, wherein Q is four.

19. (Original) The circuit of Claim 11, wherein Q is four.

20. (Original) The circuit of Claim 11, wherein:

the unaligned data stream conforms to a SONET communications standard;

the predetermined byte value is A2 as defined by the SONET standard; and

the predetermined sequence of byte values is A1_A1_A2_A2 as defined by the SONET standard.

21. (Original) A multi-level comma detection and alignment circuit, comprising:

a first pipeline register comprising a first series of byte-wide registers each comprising N bits, the first pipeline register comprising a plurality of data input terminals, M byte-wide output terminals, and a plurality of bit-wide output terminals, wherein N and M are integers;

a first compare circuit having M byte-wide input terminals coupled to the M byte-wide output terminals of the first pipeline register and further having a plurality of output terminals;

a first alignment control circuit having a plurality of input terminals coupled to the output terminals of the first compare circuit and further having a plurality of select output terminals;

a first multiplexer circuit having a plurality of data input terminals coupled to the bit-wide output terminals of the first pipeline register, a plurality of select input terminals coupled to the select output terminals of the first alignment control circuit, and a plurality of output terminals;

a second pipeline register comprising a second series of byte-wide registers each comprising N bits, the second pipeline register comprising a plurality of input terminals coupled to the output terminals of the first multiplexer circuit, P first byte-wide output terminals, and Q second byte-wide output terminals, wherein P and Q are integers;

a second compare circuit having P byte-wide input terminals coupled to the P first byte-wide output terminals of the second pipeline register and further having a plurality of output terminals;

a second alignment control circuit having a plurality of input terminals coupled to the output terminals of the second compare circuit and further having a plurality of select output terminals;

a second multiplexer circuit having Q byte-wide data input terminals coupled to the Q second byte-wide output terminals of the second pipeline register, a plurality of select input terminals coupled to the select output terminals of the second alignment control circuit, and a plurality of output terminals; and

an aligned data stream register having a plurality of input terminals coupled to the output terminals of the second multiplexer circuit and further having a plurality of output terminals.

22. (Original) The circuit of Claim 21, further comprising:

a partially aligned data stream register having a plurality of input terminals and a plurality of output terminals, the partially aligned data stream register being coupled between the output terminals of the first multiplexer circuit and the input terminals of the second pipeline register.

23. (Original) The circuit of Claim 21, wherein N is eight.

24. (Original) The circuit of Claim 23, wherein M is five, P is seven, and Q is four.

25. (Original) The circuit of Claim 21, wherein M is five.

26. (Original) The circuit of Claim 21, wherein P is seven.

27. (Original) The circuit of Claim 21, wherein Q is four.